Synthesizer Reference (623-2085-001)

Rockwell International

instructions

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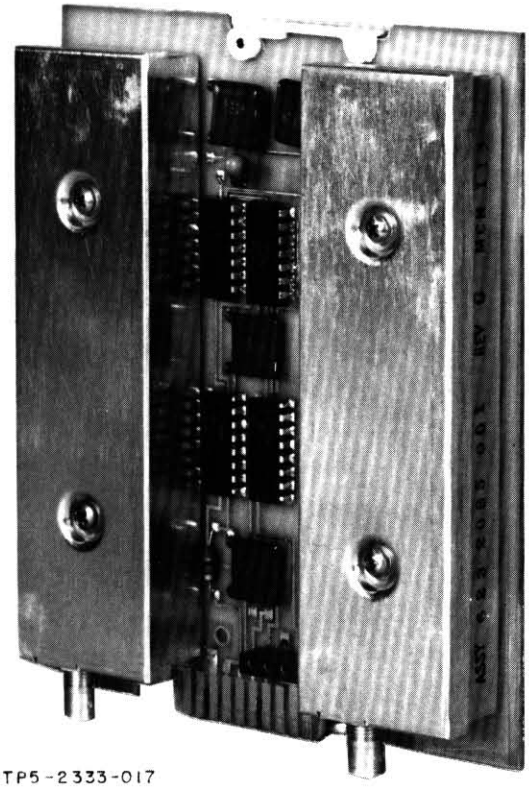
1. DESCRIPTION

Synthesizer Reference 623-2085-001, shown in figure 1, is a module that contains a base 3-layer planar card and two rf secure compartments (metal box construction) that contain two printed wiring boards. It has provisions for mounting an external phase-lock card that is used with an external frequency standard. The base 3-layer planar card contains a 20-pin, edge-on connector (2 layers, 10 pins each).



TP5-2333-017

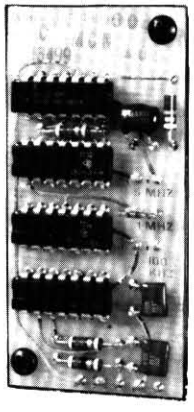
Synthesizer Reference
Figure 1

The synthesizer reference module consists of a reference oscillator, a times 12 multiplier, a divide-by-11 circuit, a divide-by-9 circuit, a divide-by-2 circuit, and provisions for using the optional external phase-lock card.

1.1 External Phase-Lock (Optional)

External Phase-Lock 635-0655-001, shown in figure 2, is an optional printed wiring board that mounts to the synthesizer reference module and allows an external frequency standard to be used. The external phase-lock card is a 2-layer planar card that uses a 5-pin connector to mate with the synthesizer reference module.

The external phase-lock card consists of a squaring amplifier, a divide-by-10 circuit, a divide-by-5 circuit, a phase discriminator, and provisions to allow using a 100-kHz, 1-MHz, or 5-MHz external frequency standard.



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External Phase-Lock
Figure 2

NOTICE: This section replaces first edition dated 1 June 1977.

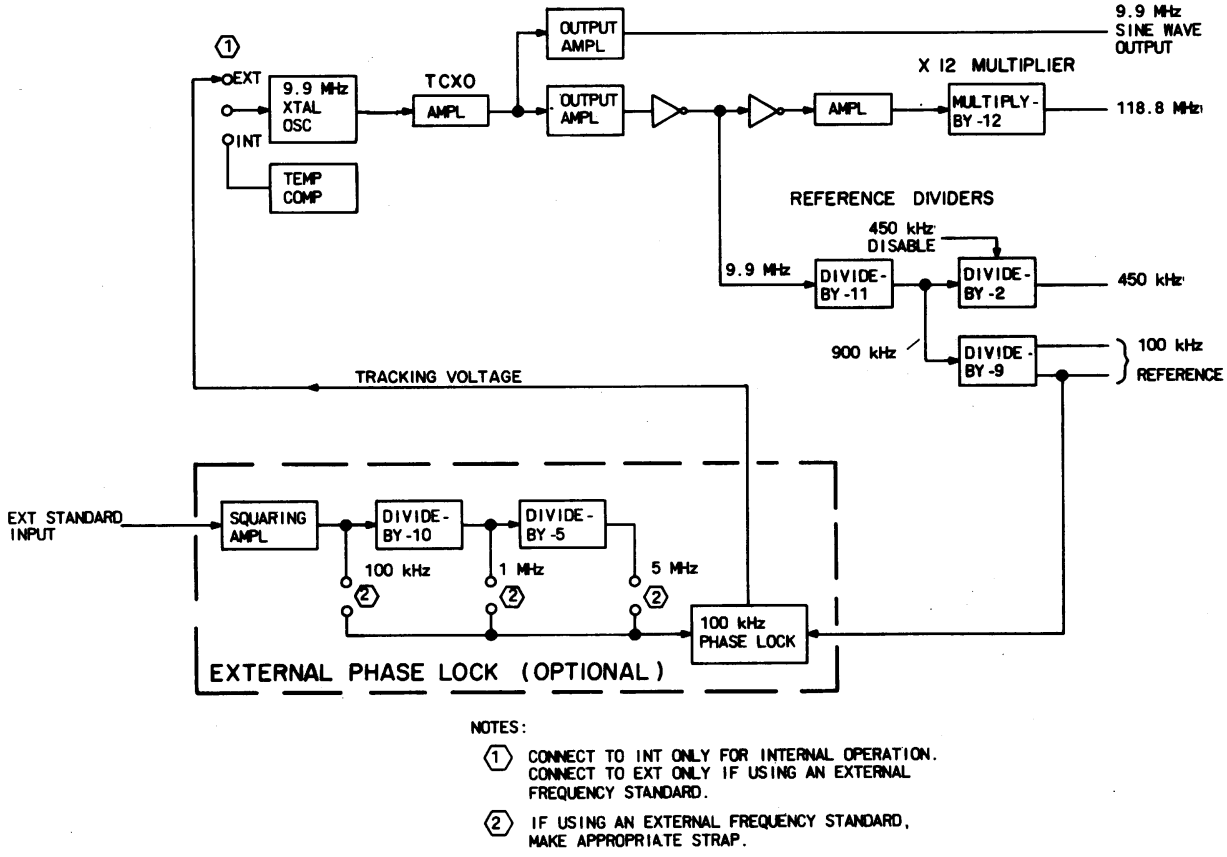
2. PRINCIPLES OF OPERATION

2.1 General (Refer to figure 3.)

The synthesizer reference module receives input voltages and a 450-kHz enable/disable signal and generates a 9.9-MHz sine-wave output, a 118.8-MHz output, a 450-kHz output, and a 100-kHz reference signal output. The 9.9-MHz, 118.8-MHz, and 450-kHz outputs are used as injection inputs to the rf translator and if amplifiers, and the 100-kHz output is used as a reference for generating the variable injection frequencies. In addition, if the external phase-lock card is used, the synthesizer reference module outputs are frequency/temperature stabilized by an external 100-kHz, 1-MHz, or 5-MHz frequency standard.

2.2 TCXO (Refer to figure 9.)

The tcxo is a voltage-controlled, temperature-compensated crystal oscillator. When used with its internal compensation circuit, RT1 through RT3 provide a temperature-compensated voltage control signal to the crystal oscillator. The crystal oscillator supplies a 9.9-MHz signal through one output amplifier to the rf translator for fixed 9.9-MHz signal



NOTES:

1. CONNECT TO INT ONLY FOR INTERNAL OPERATION. CONNECT TO EXT ONLY IF USING AN EXTERNAL FREQUENCY STANDARD.
2. IF USING AN EXTERNAL FREQUENCY STANDARD, MAKE APPROPRIATE STRAP.

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Synthesizer Reference, Block Diagram
Figure 3

injection. The crystal oscillator supplies the 9.9-MHz signal through a second output amplifier to an inverter.

The 9.9-MHz signal from the inverter is supplied to the reference dividers and through a second inverter to the times 12 multiplier.

2.3 Times 12 Multiplier (Refer to figure 9.)

The 9.9-MHz signal is received by the times 12 multiplier, multiplied and applied to crystal filter Y1 (118.8 MHz), and produces an output 12 times the frequency of the applied input. The 118.8-MHz output is supplied to the rf translator for fixed 118.8-MHz signal injection.

2.4 Reference Dividers (Refer to figure 9.)

2.4.1 Divide-by-11

The 9.9-MHz signal is received by the divide-by-11 circuit, divided (900 kHz), and applied to the divide-by-9 and divide-by-2 circuits. The divide-by-11 circuit consists of an up/down decade counter and a D-type flip-flop. Refer to table 1 for the logic truth table of the divide-by-11 circuit. Note that when the ripple clock (cc) output resets the D-type flip-flop, it latches the reset condition until the ripple clock is removed (after the next clock input). This causes the decade counter to be loaded at counter 0 for the last half of clock 9, all of clock 10, and until after clock 11 is applied; then the load (L) logic 0 is removed. Clock 12 and clock 1 are one and the same, producing a divide-by-11 circuit.

2.4.2 Divide-by-9

The 900-kHz signal from the divide-by-11 circuit is received by the divide-by-9 circuit, divided (100 kHz), and applied as a 100-kHz reference signal to the unit under control and the external phase lock (if used). The divide-by-9 circuit consists of an up/down decade counter. Refer to table 2 for a logic truth table of the divide-by-9 circuit. Note that the ripple clock (RC) output loads the decade counter to count 0 during the last half of clock 9 and allows the counter to count 1 at

Table 1. Divide-by-11 Logic Truth Table.

CLOCK INPUT	U1						U3A				
	OUTPUTS						INPUTS			OUTPUTS	
	QA	QB	QC	QD	RC	COUNT	C	D	R	Q	$\overline{Q}$
1	1	0	0	0	1	1	1	1	1	1	0
2	0	1	0	0	1	2	2	1	1	1	0
3	1	1	0	0	1	3	3	1	1	1	0
4	0	0	1	0	1	4	4	1	1	1	0
5	1	0	1	0	1	5	5	1	1	1	0
6	0	1	1	0	1	6	6	1	1	1	0
7	1	1	1	0	1	7	7	1	1	1	0
8	0	0	0	1	1	8	8	1	1	1	0
9	1	0	0	1	1	9	9	1	1	1	0
9.5	0	0	0	0	*0	0	9.5	0	0	0	1
10	0	0	0	0	1	0	10	1	1	0	1
11	0	0	0	0	1	0	11	1	1	1	0
12/1	1	0	0	0	1	1	12/1	1	1	1	0

*RC logic 0 appears only for one-half clock cycle time and returns to logic 1 (U1 is reset to start count at 1).

Table 2. Divide-by-9 Logic Truth Table.

CLOCK INPUT	U2					
	OUTPUTS					
	QA	QB	QC	QD	RC	COUNT
1	1	0	0	0	1	1
2	0	1	0	0	1	2
3	1	1	0	0	1	3
4	0	0	1	0	1	4
5	1	0	1	0	1	5
6	0	1	1	0	1	6
7	1	1	1	0	1	7
8	0	0	0	1	1	8
9	1	0	0	1	1	9
9.5	0	0	0	0	*0	0
10/1	1	0	0	0	1	1

*RC logic 0 appears only for one-half clock cycle time and returns to logic 1 (U1 is reset to start count at 1).

clock 10. Clock 10 and clock 1 are one and the same, producing a divide-by-9 circuit.

2.4.3 Divide-by-2

The 900-kHz signal from the divide-by-11 circuit is received by the divide-by-2 circuit, divided (450 kHz), and applied as a 450-kHz carrier reinsertion signal to the unit under control. The divide-by-2 circuit consists of a D-type flip-flop. Refer to table 3 for a logic truth table of the divide-by-2 circuit. Note that a logic 0 on the set input disables the divide-by-2 circuit (latches it in the set condition).

2.5 External Phase-Lock (Refer to figure 10.)

The external phase-lock card receives an external frequency standard (5 MHz, 1 MHz, or 100 kHz) and a tcxo 100-kHz reference signal for use in generation of a tracking voltage output for control of the synthesizer reference tcxo. The external phase lock must be internally strapped for the appropriate external frequency standard.

Table 3. Divide-by-2, Logic Truth Table.

INPUTS			OUTPUTS	
Clock	D	S	Q	$\overline{Q}$
⟶1	0	1	0	1
No change	1	1	No change	
⟶1	1	1	1	0
No change	0	1	No change	
⟶1	0	1	0	1
X	X	0	1	0

⟶1 = change from logic 0 to logic 1
1 = logic 1
0 = logic 0
X = no effect

2.5.1 100-kHz External Standard

When a 100-kHz external standard is used, it is supplied through the squaring amplifier to the phase detector. A 100-kHz internal reference standard is also applied to the phase detector. The 100-kHz signals are phase compared and a resultant tcxo dc input signal is supplied by the external phase lock.

2.5.2 1-MHz External Standard

When a 1-MHz external standard is used, it is supplied through squaring amplifier to the divide-by-10 circuit. The 100-kHz output of the divide-by-10 circuit is supplied as a 100-kHz external standard to the phase detector. Refer to paragraph 2.5.1 for operation using the 100-kHz external standard.

The divide-by-10 circuit uses a decade counter consisting of a divide-by-2 and a divide-by-5 counter connected to produce a divide-by-10 circuit. Refer to paragraph 2.7 for details on this decade counter.

2.5.3 5-MHz External Standard

When a 5-MHz external standard is used, it is supplied through squaring amplifier to divide-by-10 circuit. The 500-kHz output of the divide-by-10 circuit is supplied to the divide-by-5 circuit, and the 100-kHz output of the divide-by-5 circuit is supplied as a 100-kHz external standard to the phase detector. Refer to paragraph 2.5.1 for operation using the 100-kHz external standard.

The divide-by-10 and divide-by-5 circuits use decade counters consisting of a divide-by-2 and a divide-by-5 counter connected to produce divide-by-10 and divide-by-5 circuits. Refer to paragraph 2.7 for details on this decade counter.

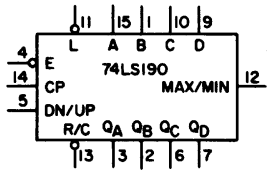
2.6 Up/Down Decade Counter 74LS190 (Refer to figure 4.)

The up/down decade counters used in the synthesizer reference module are provided with an enable control presetting facility, single line up/down control, cascading for multidecade operation, and buffered inputs. The 74LS190 is a 4-bit decade counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when input conditions are met. This mode of operation will eliminate the output counting spikes that are normally associated with asynchronous (ripple clock) counters.

A high at the enable input inhibits counting. A low at the enable input and a low-to-high clock transition triggers the four master/slave flip-flops. The enable input should be changed only when the clock is high. The down/up input determines the direction of the count. When low, the count goes up; when high, the count goes down.

These counters are fully programmable. The outputs may be preset to any state by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the state of the clock input. This feature allows the counters to be used as modulo N dividers by simply modifying the count length with the preset inputs.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low level output pulse equal in width to the low level portion of the clock input when an overflow or underflow condition exists. The counters can be cascaded easily by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.



Up/Down Decade Counter 74LS190
Figure 4

Table 4. Up/Down Decade Counter 74LS190, Logic Truth Table.

PROGRAMMABLE INPUTS				COUNT	BCD OUTPUTS			
A	B	C	D		QA	QB	QC	QD
0	0	0	0	0	0	0	0	0
1	0	0	0	1	1	0	0	0
0	1	0	0	2	0	1	0	0
1	1	0	0	3	1	1	0	0
0	0	1	0	4	0	0	1	0
1	0	1	0	5	1	0	1	0
0	1	1	0	6	0	1	1	0
1	1	1	0	7	1	1	1	0
0	0	0	1	8	0	0	0	1
1	0	0	1	9	1	0	0	1

E (enable): logic 0 enables counter; logic 1 inhibits counter.

L (load): logic 0 programs the bcd output count to be set at the bcd count of the programmable inputs; the next clock pulse counts one higher/lower (up/down).

DU (down/up): logic 0 counts up; logic 1 counts down.

CP (clock pulse): logic 0-to-logic 1 transition advances counter.

RC (ripple clock): logic 0 pulse equal to 1/2 clock cycle when an overflow occurs.

MM (maximum/minimum count): logic 1 pulse equal to full clock cycle when an overflow or underflow occurs.

2.7 Decade Counter 74LS90 (Refer to table 5.)

The 74LS90 used in the external phase-lock card is a high-speed, monolithic decade counter consisting of

four dual-rank, master-slave flip-flops internally interconnected to provide a divide-by-2 counter and a divide-by-5 counter. Gated direct reset lines are provided to inhibit count inputs and return all outputs to a logic 0 or to a binary coded decimal (bcd) count of 9. As the output from flip-flop A is not internally connected to the succeeding stages, the count may be separated into the three following independent count modes:

a. When used as a binary coded decimal decade counter, the BD input must be externally connected to the A output. The A input receives the incoming count, and a count sequence is obtained in accordance with the bcd count sequence truth table shown above. In addition to a conventional 0 reset, inputs are provided to reset a bcd 9-count for 9's complement decimal applications.

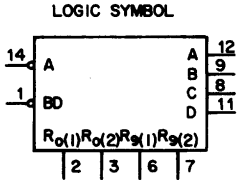
Table 5. Decade Counter 74LS90, Logic Truth Table.

*BCD COUNT SEQUENCE				
COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

**RESET/COUNT							
RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	D	C	B	A
1	1	0	X	0	0	0	0
1	1	X	0	0	0	0	0
X	X	1	1	1	0	0	1
X	0	X	0	Count			
0	X	0	X	Count			
0	X	X	0	Count			
X	0	0	X	Count			

*Output A connected to input BD for BCD count.
**X indicates that either a logical 1 or a logical 0 may be present.

b. If a symmetrical divide-by-10 count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of 10, the D output must be externally connected to the A input. The input count is then applied at the BD input and a divide-by-10 square wave is obtained at output A.
c. For operation as a divide-by-2 counter and a divide-by-5 counter, no external connections are required. Flip-flop A is used as a binary element for the divide-by-2 function. The BD input is used to obtain binary divide-by-5 operation at the B, C, and D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.



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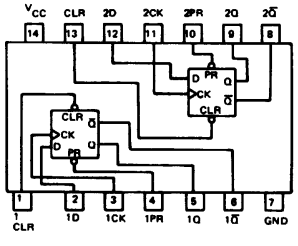
Decade Counter 74LS90
Figure 5

2.8 Dual D-Type Flip-Flop With Preset and Clear 74LS74 (Refer to table 6.)

The 74LS74 consists of dual high-speed, D-type flip-flops. Information at D input is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either high or low level, the D-input signal has no effect.



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Dual D-Type Flip-Flop With Preset and Clear 74LS74
Figure 6

Table 6. Dual D-Type Flip-Flop With Preset and Clear 74LS74, Logic Truth Table.

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	*H	*H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_o	$\overline{Q_o}$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_o = the level of Q before the indicated input conditions were established.
* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

3. TESTING/TROUBLESHOOTING PROCEDURES

3.1 Test Equipment and Power Requirements

Test equipment and power sources required to test, troubleshoot, and repair the synthesizer reference module are listed in the maintenance section of this instruction book.

3.2 Testing

The test procedures in table 7 check total performance of the synthesizer reference. The test procedures in table 8 check total performance of the external phase-lock. These test procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.

Table 7. Synthesizer Reference, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	a. Remove top cover of the unit containing the synthesizer reference that is to be tested.		
	b. Remove cover from the synthesizer section of the unit.		
	c. Remove synthesizer reference and install it on an extender card and place it in the unit.		
	d. Set unit LINE SELECTOR switch to 115 V.		
	e. Connect unit to 115-V ac power source and set power on.		
	f. Measure dc voltage from J1-14 and J1-4 to J1-9 (ground).	+5.2 ±0.2 V dc.	Check unit synthesizer voltage regulator.
	g. Measure dc voltage from J1-12 to J1-9 (ground).	NLT +19.5 V dc, NMT +20.8 V dc.	Check unit synthesizer voltage regulator.
	h. Set unit MODE switch to ISB.		
2. 100-kHz reference outputs	a. Using a frequency counter, measure the output between J1-17 and J1-18 (ground).	100 ±0.1 kHz.	
	b. Using an oscilloscope, check the square-wave outputs of J1-17 and J1-18 (ground).	Negative swing (logic 0) is NMT 0.5 V dc. Positive swing (logic 1) is NLT +3.0 V dc.	
(Cont)			

Table 7. Synthesizer Reference, Testing and Troubleshooting Procedures (Cont).

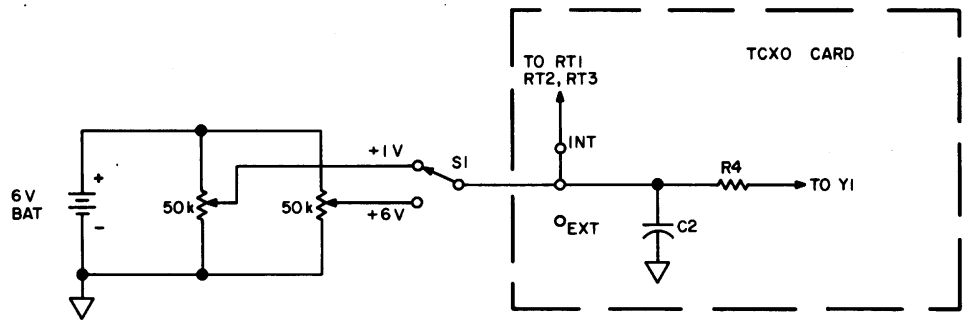
TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	c. Using a frequency counter, measure the output between J1-15 and J1-18 (ground).		
	d. Using an oscilloscope, check the square-wave outputs at J1-15 and J1-18 (ground).	Negative swing (logic 0) is NMT 0.5 V dc. Positive swing (logic 1) is NLT +3.0 V dc.	
3. 450-kHz sine-wave output	a. Using an rf voltmeter with a 50-ohm adapter, measure the output between J1-6 and J1-7 (ground).	300 ±75 mV rms.	Check U3B and associated circuit.
	b. Set unit MODE switch to AM.		
	c. Note the output between J1-6 and J1-7 (ground).	≅ 0 mV rms.	Check U3B and unit 450-kHz disable circuit.
	d. Set unit MODE switch to ISB.		
	e. Using a frequency counter, measure the output between J1-6 and J1-7 (ground).	450 ±0.5 kHz.	Check U3A, U3B, and associated circuit.
4. 118.8-MHz sine-wave output	a. Remove shield that covers Y2 (refer to figure 9).		
	b. Using an rf voltmeter with an unloaded probe tip, measure the rf voltage at Y2 output.	Note output.	
	c. Adjust C24 and C28 for maximum output.		
	d. Using an rf voltmeter with a 50-ohm adapter measure the output at P2.		
	e. Adjust C32, C24, and C28 for maximum output.		
	f. Note level after C32, C24, and C28 adjustment.	500 ±100 mV rms.	Adjust A2R27 for 500 mV rms or A2C32 for 500 mV rms if A2R27 not installed.
5. 9.9-MHz sine-wave output (Cont)	a. Using an rf voltmeter with a 50-ohm adapter, measure the output at P3.	300 ±75 mV rms.	Adjust A1R20 for 300-mV rms output. Check that tcxo is strapped to INT. If the above does not correct the results replace A1 tcxo card. (Return tcxo card to factory for repair.)

Table 7. Synthesizer Reference, Testing and Troubleshooting Procedures (Cont).

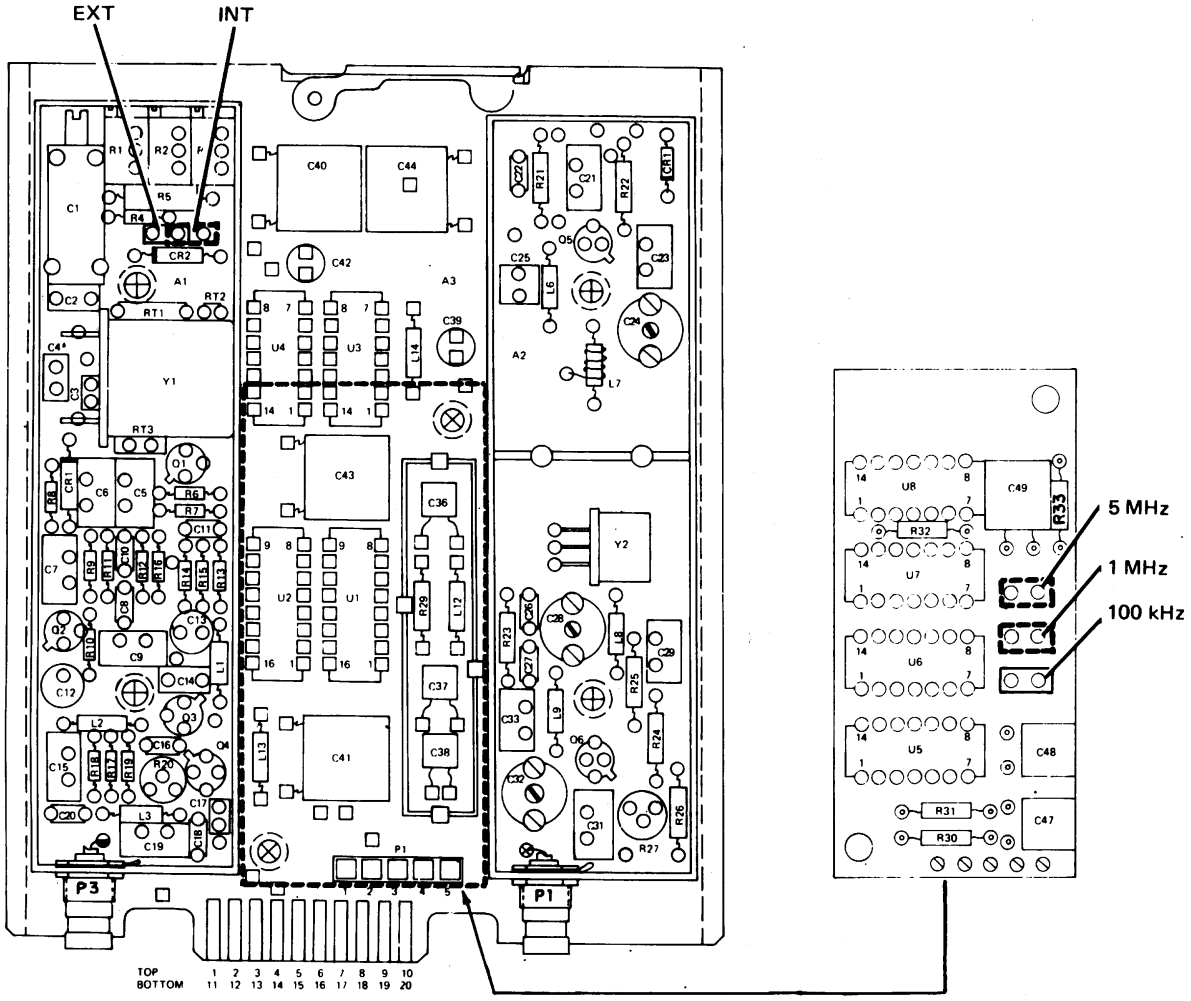
TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. (Cont)	***Note*** Field repair of the tcxo card is not recommended; however, if field repair must be accomplished the following additional items of test equipment are required to ensure proper testing and operation. a. Frequency counter, Fluke 1980A (1-Hz accuracy). b. Temperature box, Delta Design MN2800. c. Bias adjustment test box (fabricate per figure 7).		
6. Tcxo card test procedures	***Note*** If strong rf fields are present, shielding may be required to meet accuracy requirements.		
	a. Using an oscilloscope with a high-impedance probe, measure the output waveform at Q3-C.	9.9-MHz square wave, symmetrical to with 20%. (Duration of longest half cycle of square wave may not exceed shortest half cycle by more than 20%.)	Check Q1, Q2, Q3, Y1, and associated circuit.
	b. Note the output voltages at Q3-C.	Negative swing (logic 0) is NMT 0.5 V dc. Positive swing (logic 1) is NLT +3.5 V dc.	Check Q3 and associated circuit.
	c. Using an rf voltmeter with a 50-ohm adapter measure the output at P3.	300 ±75 mV rms.	Adjust A1R20 for 300-mV rms output. Check Q2, Q4, and associated circuit.
	d. Connect bias for frequency adjustment using setup in figure 7.		
	e. Adjust +1-V bias control for +2.5 V dc.		
	f. Using the frequency counter, measure the output at P3.	9.9 MHz ±10 Hz.	Select a value of C4 from those listed in parts list to produce 9.9 MHz ±10 Hz. ***Note*** C1 must be adjustable from 9.9 MHz -10 Hz through 9.9 MHz +10 Hz. If not, select value of C4 to meet this requirement.
(Cont)			

Table 7. Synthesizer Reference, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
6. (Cont)	g. Adjust +1-V bias control for +1.0 V dc.		
	h. Using the frequency counter, measure the output at P3 with the bias set at the +1 V position and with the bias set at the +6 V position.	Note frequency at each bias setting. Sensitivity should be 400 to 550 Hz. (Sensitivity is the difference between the two frequencies.	Select a value of C3 from those listed in parts list to produce 400- to 550-Hz sensitivity. Step f should be repeated if value of C3 is changed.
	i. Remove bias from test setup.		
	j. Using a dvm, check dc bias at R4-C2 junction. (Refer to figures 7 and 8.)	+2.1 to +2.5 V dc.	Adjust R1, R2, and R3 to nominal values. Adjust R3 for +2.5 V dc at R4-C2 junction.
	k. Place tcxo in temperature box.		
	l. Decrease temperature to 0 °C (+32 °F). Allow time for tcxo to stabilize at this temperature.		
	m. Using the frequency counter, measure the output at P3.	9.9 MHz ±4.0 Hz.	Adjust R2 for 9.9 MHz ±1.0 Hz.
	n. Increase temperature to +25 °C (+77 °F).		
	o. Using the frequency counter, measure the output at P3.	9.9 MHz ±4.0 Hz.	Adjust R3 for 9.9 MHz ±1.0 Hz.
	p. Increase temperature to +75 °C (+167 °F).		
	q. Using the frequency counter, measure the output at P3.	9.9 MHz ±4.0 Hz.	Adjust R1 for 9.9 MHz ±1.0 Hz.
	r. If any adjustments are made repeat steps k thru q.	Continue to step s.	If after several tries adjustment fails to pass at all temperature levels, check RT1, RT2, RT3, Y1, and associated circuit.
	s. Using the frequency counter, measure the output at P3 at each of the following temperatures (allow the tcxo to stabilize at each temperature). 0 °C (+32 °F) +10 °C (+50 °F) +25 °C (+77 °F) +45 °C (+113 °F) +60 °C (+140 °F) +70 °C (+158 °F) +75 °C (+167 °F)	9.9 MHz ±4.0 Hz.	Perform adjustments in steps k thru q. If after several tries adjustment fails to pass at all temperature levels, check RT1, RT2, RT3, Y1, and associated circuit.
	t. Remove tcxo from temperature box and reinstall in unit.		



Frequency Adjustment Bias, Test Setup
Figure 7



Strapping for External Frequency Standard
Figure 8

Table 8. External Phase-Lock, Testing and Troubleshooting Rrocedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	a. Remove top cover of the unit containing the external phase-lock that is to be tested.		
	b. Remove cover from the synthesizer section of the unit.		
	c. Remove synthesizer reference (with external phase-lock) and install it on an extender card and place it in the unit.		
	d. Set unit LINE SELECTOR switch to 115 V.		
	e. Connect unit to 115-V ac power source and set power on.		
	f. Measure dc voltage from external phase-lock P1-4 to P1-2 (ground).	+5.2 ±0.2 V dc.	Check unit synthesizer voltage regulator and associated synthesizer reference.
	Note Clip inside tcxo must be in the external position (refer to figure 8).		
2. 5-MHz external reference	a. Set clip on the external phase-lock to the 5-MHz position.		
	b. Connect 5-MHz external standard (0.5 to 1.5 V rms) to J23 EXT STD jack on unit.		
	c. Connect an oscilloscope to U8-8 and observe square wave.	Steady duty ratio, indicating locked condition.	Check U5, U6, U7, and U8.
	d. Ground P1-5 and observe square wave at U8-8.	Unsteady square wave.	Check U8.
	e. Remove P1-5 ground and observe square wave at U8-8.	Steady duty ratio, indicating locked condition.	Check U5, U6, U7, and U8.
3. 1-MHz external reference.	a. Set clip on the external phase-lock to the 1-MHz position.		
	b. Connect 1-MHz external standard (0.5 to 1.5 V rms) to J23 EXT STD jack on unit.		
	c. Connect an oscilloscope to U8-8 and observe square wave.	Steady duty ratio, indicating locked condition.	Check U5, U6, and U8.
	d. Ground P1-5 and observe square wave at U8-8.	Unsteady square wave.	Check U8.
	e. Remove P1-5 ground and observe square wave at U8-8.	Steady duty ratio, indicating locked condition.	Check U5, U6, and U8.

Table 8. External Phase-Lock, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. 100-kHz external reference	a. Set clip on the external phase lock to the 100-kHz position.		
	b. Connect 100-kHz external standard (0.5 to 1.5 V rms) to J23 EXT STD jack on unit.		
	c. Connect an oscilloscope to U8-8 and observe square wave.	Steady duty ratio, indicating locked condition.	Check U5 and U8.
	d. Ground P1-5 and observe square wave at U8-8.	Unsteady square wave.	Check U8.
	e. Remove P1-5 ground and observe square wave at U8-8.	Steady duty ratio, indicating locked condition.	Check U5 and U8.

4. REPAIR

Repair of the synthesizer reference module is accomplished using the standard planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

5. PARTS LIST/DIAGRAMS

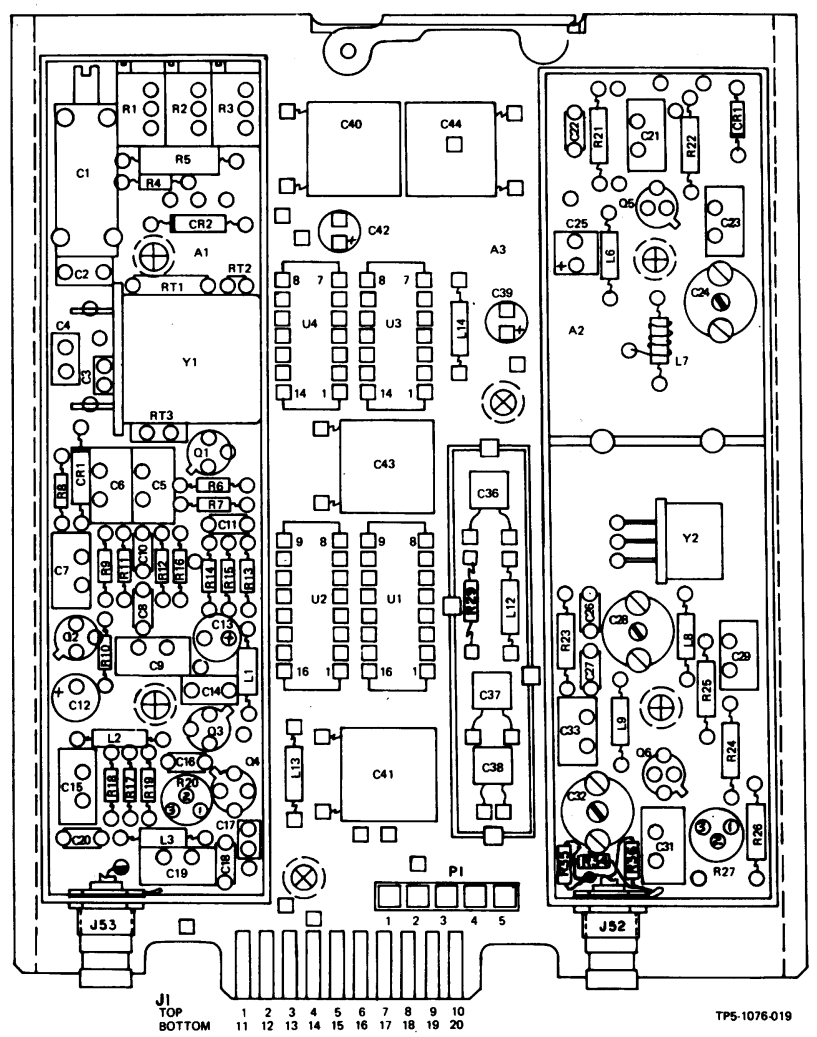
This paragraph assists in identification, requisition, and issuance of parts and in maintenance of the equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram (figures 9 and 10). The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

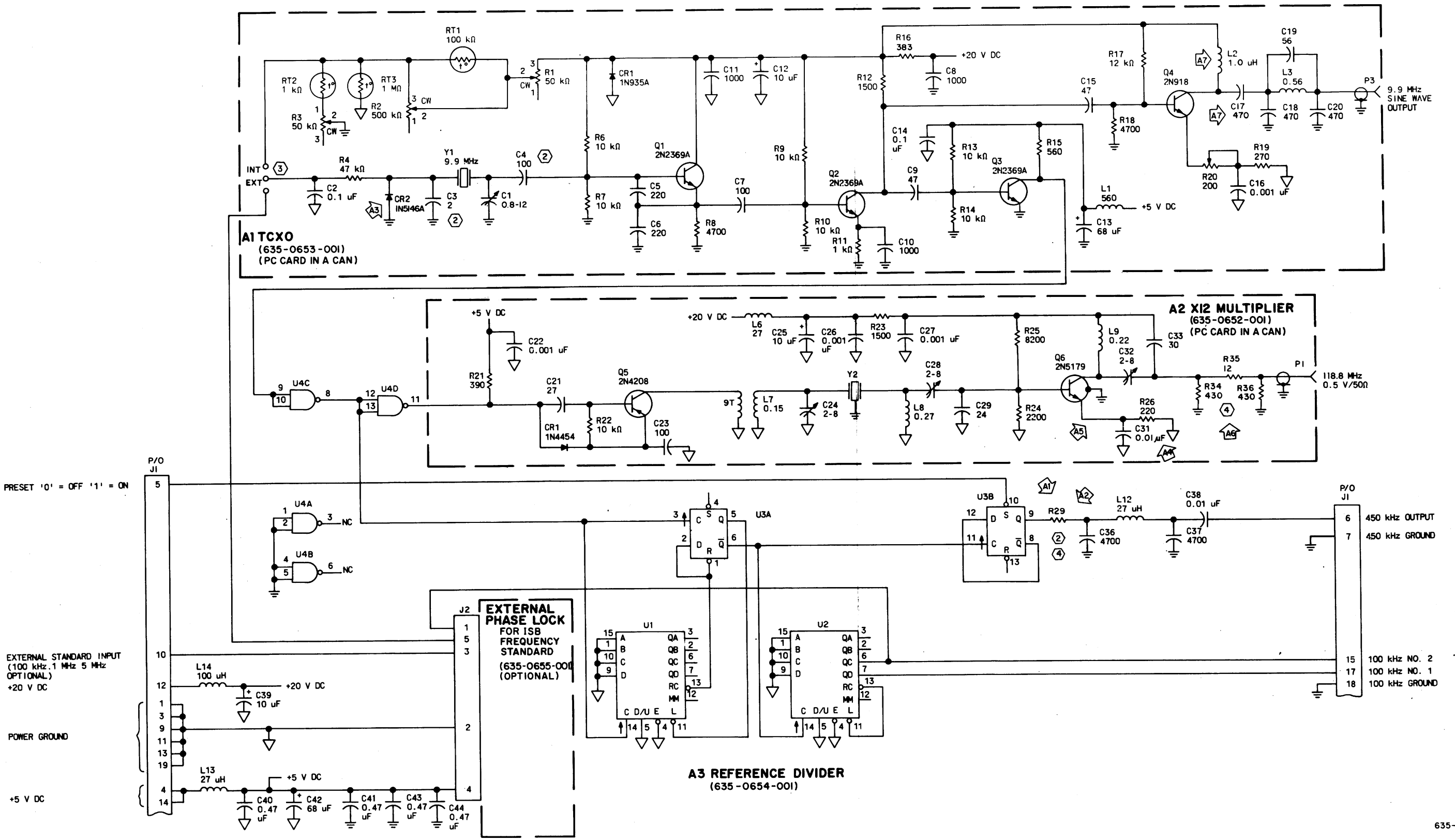
Use the reference designator indicated on schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description are listed for each reference designator.

Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses and on the schematic diagram inside an arrow that points at the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
Synthesizer reference	623-2085-001	REV E
Times 12 multiplier A2	635-0652-001	REV H
Tcxo A1	635-0653-001	REV D
Reference divider A3	635-0654-001	REV G
External phase-lock (optional)	635-0655-001	REV D





Synthesizer Reference, Schematic Diagram
Figure 9 (Sheet 1 of 2)

PARTS LIST

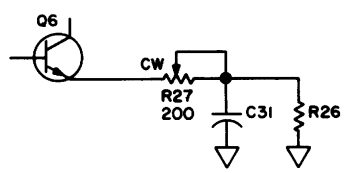
REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
	SYNTHESIZER REFERENCE 623-2085-001		
A1	TCXO	635-0653-001	
A2	X12 MULTIPLIER	635-0652-001	
A3	REFERENCE DIVIDER	635-0654-001	
J1-J51	NOT USED		
J52, J53	CONNECTOR, RCPT, ELEC	357-7207-090	
R1-R28	NOT USED		
R29	RESISTOR, FXD, CMPSN (A2) 56Ω thru 180Ω, 5%, 1/4W	635-8926-001	
R30-R33	NOT USED		
R34	RESISTOR, FXD, CMPSN, (A6) 430Ω, 5%, 1/8W	745-1863-400	
R35	RESISTOR, FXD, CMPSN, (A6) 12Ω, 10%, 1/8W	745-2271-000	
R36	RESISTOR, FXD, CMPSN, (A6) 430Ω, 5%, 1/8W	745-1863-400	
	TCXO A1 635-0653-001		
CR1	SEMICOND DEVICE, 1N935A	353-3157-000	
CR2	SEMICOND DEVICE, 1N5147 (A3)	922-6095-170	
CR2	SEMICOND DEVICE, 1N5146A	922-6095-160	
C1	CAPACITOR, VAR, GL DIEL, 0.8 TO 12pF, 750V	922-0487-000	
C2	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C3	CAPACITOR, FXD, CER DIEL, 1.2 THRU 10pF, 5%, 75V	801-3486-001	
C4	CAPACITOR, FXD, MICA DIEL, 82 THRU 220pF, 5%, 50V	801-3485-001	
C5, C6	CAPACITOR, FXD, MICA DIEL, 220pF, 5%, 500V	912-3903-000	
C7	CAPACITOR, FXD, MICA DIEL, 100pF, 5%, 500V	912-3879-000	
C8	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C9	CAPACITOR, FXD, MICA DIEL, 47pF, 5%, 500V	912-3856-000	
C10, C11	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C12	CAPACITOR, FXD, ELCTLT, 10μF, 20%, 25V	184-9102-240	
C13	CAPACITOR, FXD, ELCTLT, 68μF, 20%, 6V	184-9102-040	
C14	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C15	CAPACITOR, FXD, MICA DIEL, 47pF, 5%, 500V	912-3856-000	
C16	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C17	CAPACITOR, FXD, CER DIEL (A7) 0.01μF, 20%, 50V	913-3279-110	
C17	CAPACITOR, FXD, CER DIEL, 470pF, 10%, 200V	913-4014-000	
C18	CAPACITOR, FXD, CER DIEL, 470pF, 10%, 200V	913-4014-000	
C19	CAPACITOR, FXD, MICA DIEL, 56pF, 5%, 500V	912-3861-000	
C20	CAPACITOR, FXD, CER DIEL, 470pF, 10%, 200V	913-4014-000	
L1	COIL, RF, 560μH	240-2073-050	
L2	COIL, RF, 180μH (A7)	240-2026-000	
L2	COIL, RF, 1.0μH	240-2023-000	
L3	COIL, RF, 0.56μH	240-2020-000	
Q1-Q3	TRANSISTOR, 2N2369A	352-0596-030	
Q4	TRANSISTOR, 2N918	352-0440-000	
RT1	RESISTOR, THRM, 100kΩ, 10%, 4MW	714-1138-010	
RT2	RESISTOR, THRM, 1kΩ, 10%, 2.6MW	714-1138-060	
RT3	RESISTOR, THRM, 1MΩ, 5%, 5.3MW	714-2853-000	
R1	RESISTOR, VAR, 50kΩ, 10%, 1/2W	380-9086-030	
R2	RESISTOR, VAR, 500kΩ, 10%, 1/2W	382-1405-290	
R2	RESISTOR, VAR, 500kΩ, 10%, 1/2W	380-9086-040	
R3	RESISTOR, VAR, 50kΩ, (A), 10%, 1/2W	382-1405-250	
R3	RESISTOR, VAR, 50kΩ, 10%, 1/2W	380-9086-030	
R4	RESISTOR, FXD, CMPSN, 47kΩ, 10%, 1/8W	745-2401-000	
R5	NOT USED		
R6, R7	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/8W	745-2377-000	
R8	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/8W	745-2365-000	
R9, R10	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/8W	745-2377-000	
R11	RESISTOR, FXD, CMPSN, 1kΩ, 10%, 1/8W	745-2341-000	
R12	RESISTOR, FXD, CMPSN, 1.5kΩ, 10%, 1/8W	745-2347-000	
R13, R14	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/8W	745-2377-000	
R15	RESISTOR, FXD, CMPSN, 560Ω, 10%, 1/8W	745-2332-000	
R16	RESISTOR, FXD, WW, 383Ω, 10%, 1W	747-2183-570	
R17	RESISTOR, FXD, CMPSN, 12kΩ, 10%, 1/8W	745-2380-000	
R18	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/8W	745-2365-000	
R19	RESISTOR, FXD, CMPSN, 270Ω, 10%, 1/8W	745-2320-000	

PARTS LIST (Cont)

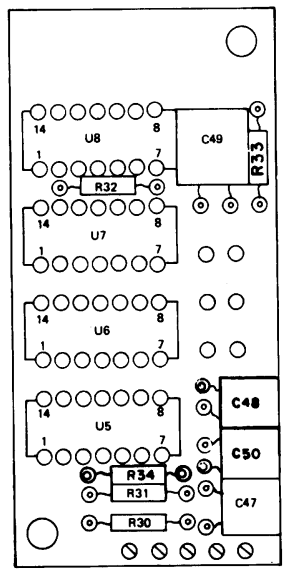
REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
R20	RESISTOR, VAR, 200Ω, 10%, 0.5W	382-0027-050	
Y1	XTAL UNIT, QTZ, 9.900000MHZ	289-7271-010	
	X12 MULTIPLIER A2 635-0652-001		
CR1	SEMICOND DEVICE, 1N4454	353-3644-010	
C1-C20	NOT USED		
C21	CAPACITOR, FXD, MICA DIEL, 27pF, 5%, 500V	912-3844-000	
C22	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C23	CAPACITOR, FXD, MICA DIEL, 100pF, 5%, 500V	912-3879-000	
C24	CAPACITOR, VAR, CER DIEL, 2 TO 8pF, 350V	917-1218-000	
C25	CAPACITOR, FXD, ELCTLT, 10μF, 20%, 25V	184-9102-240	
C26, C27	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C28	CAPACITOR, VAR, CER DIEL, 2 TO 8 pF, 350V	917-1218-000	
C29	CAPACITOR, FXD, MICA DIEL, 24pF, 5%, 500V	912-3843-000	
C30	NOT USED		
C31	CAPACITOR, FXD, MICA DIEL, (A4) 220pF, 5%, 500V	912-3903-000	
C31	CAPACITOR, FXD, CER DIEL, 0.01μF, 20%, 50V	913-3279-110	
C32	CAPACITOR, VAR, CER DIEL, 2 TO 8 pF, 350V	917-1218-000	
C33	CAPACITOR, FXD, MICA DIEL, 30pF, 5%, 500V	912-3846-000	
L1-L5	NOT USED		
L6	COIL, RF, 27μH	240-2040-000	
L7	COIL, RF, 0.15μH	637-1783-001	
L8	COIL, RF, 0.27μH	240-2016-000	
L9	COIL, RF, 0.22μH	240-2015-000	
Q1-Q4	NOT USED		
Q5	TRANSISTOR, 2N4208	352-0959-020	
Q6	TRANSISTOR, 2N5179	352-0792-020	
R1-R20	NOT USED		
R21	RESISTOR, FXD, CMPSN, 390Ω, 10%, 1/4W	745-0734-000	
R22	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R23	RESISTOR, FXD, CMPSN, 1.5kΩ, 10%, 1/4W	745-0755-000	
R24	RESISTOR, FXD, CMPSN, 2.2kΩ, 10%, 1/4W	745-0761-000	
R25	RESISTOR, FXD, CMPSN, 8.2kΩ, 10%, 1/4W	745-0782-000	
R26	RESISTOR, FXD, CMPSN, 220Ω, 10%, 1/4W	745-0725-000	
R27	RESISTOR, VAR, 200Ω, 10%, 0.5W, (A5)	382-0027-050	
Y1	NOT USED		
Y2	FILTER, XTAL, BP, 118.8MHZ	293-1315-010	
	REF DIVIDER A3 635-0654-001		
C1-C35	NOT USED		
C36, C37	CAPACITOR, FXD, CER DIEL, 4700pF, 10%, 100V	913-5019-160	
C38	CAPACITOR, FXD, CER DIEL, 0.01μF, 20%, 50V	913-3279-110	
C39	CAPACITOR, FXD, ELCTLT, 10μF, 20%, 25V	184-9102-240	
C40, C41	CAPACITOR, FXD, CER DIEL, 0.47μF, 10%, 200V	913-3279-690	
C42	CAPACITOR, FXD, ELCTLT, 68μF, 20%, 6V	184-9102-040	
C43, C44	CAPACITOR, FXD, CER DIEL, 0.47μF, 10%, 200V	913-3279-690	
L1-L11	NOT USED		
L12, L13	COIL, RF, 27μH	240-2040-000	
L14	COIL, RF, 100μH	240-2047-000	
P1	HOUSING, CONN	372-2625-014	
U1, U2	INTEGRATED CKT, SN74LS190N	351-1527-040	
U3	INTEGRATED CKT, SN74LS74N	351-1525-040	
U4	INTEGRATED CKT, 7400N	351-7629-010	

MODIFICATION HISTORY

REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
	SYNTH REF 623-2085-001	
A1	Removed A3R29, 47Ω.	635-0654-001, REV C and above
A2	Added R29, test select of 56 to 180Ω (in same location as A3R29 was removed).	623-2085-001, REV C and above
A3	Changed A1CR2 from 1N5147 to 1N5146A.	635-0653-001, REV E and above
A4	Changed A2C31 from 220pF to 0.01μF.	635-0652-001, REV C and above
A5	Removed A2R27, 200Ω variable. Circuit was as shown below.	635-0652-001, REV D and above
A6	Added R34, 430Ω. Added R35, 12Ω. Added R36, 430Ω.	623-2085-001, REV D and above
A7	Changed: C17 from 0.01μF., L2 from 1.8μH to 1.0μH.	635-0653-001, REV F and above
	EXTERNAL PHASE-LOCK 635-0655-001	
A1	Added C50, 0.1μF. Added R34, 2200Ω. Changed R31 from 4700Ω to 2200Ω.	REV C and above



Synthesizer Reference, Schematic Diagram
Figure 9 (Sheet 2)



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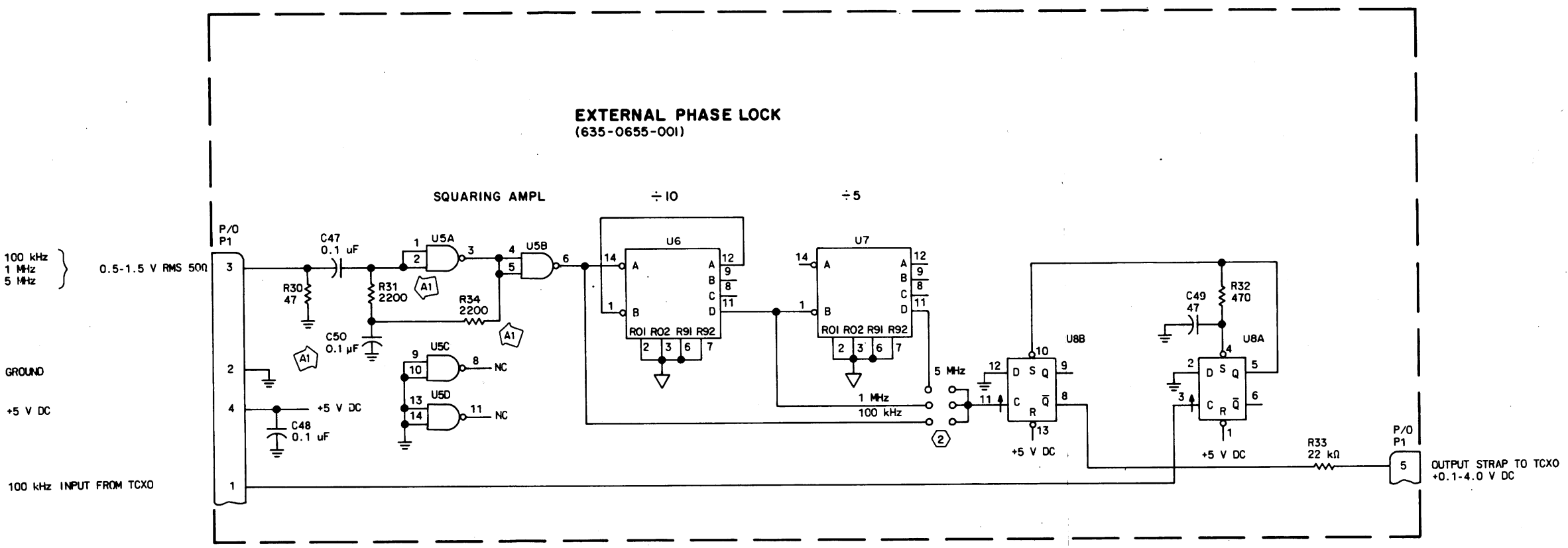

POWER AND GROUND CONNECTIONS

U NO.	TYPE	POWER (V DC)	
		+5	GND
U5	N74LS00A	14	7
U6, U7	SN74LS90N	5	10
U8	SN74LS74N	14	7

(1) UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN PICOFARADS.

(2) OPTIONAL STRAPPING CLIP.

(3) PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.

635-0430 SH 2

External Phase-Lock, Schematic Diagram
Figure 10 (Sheet 1 of 2)

PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
	EXTERNAL PHASE LOCK (OPTION) 635-0655-001		
C1-C46	NOT USED		
C47, C48	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C49	CAPACITOR, FXD, MICA DIEL, 47pF, 5%, 500V	912-3856-000	
C50	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
	(A1)		
R1-R29	NOT USED		
R30	RESISTOR, FXD, CMPSN, 47Ω, 10%, 1/4W	745-0701-000	
R31	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W	745-0773-000	
	(A1)		
R31	RESISTOR, FXD, CMPSN, 2.2kΩ, 10%, 1/4W	745-0761-000	
R32	RESISTOR, FXD, CMPSN, 470Ω, 10%, 1/4W	745-0737-000	
R33	RESISTOR, FXD, CMPSN, 22kΩ, 10%, 1/4W	745-0797-000	
R34	RESISTOR, FXD, CMPSN, 2.2kΩ, 10%, 1/4W	745-0761-000	
	(A1)		
U1-U4	NOT USED		
U5	INTEGRATED CKT, N74LS00A	351-1523-110	
U6, U7	INTEGRATED CKT, SN74LS90N	351-1636-010	
U8	INTEGRATED CKT, SN74LS74N	351-1525-040	

External Phase-Lock, Schematic Diagram
Figure 10 (Sheet 2)